CLAIMS

WE CLAIM:

1. A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

developing at least one simulation test vector using a PLD design automation software tool, each simulation test vector used to test a simulated model of the programmed PLD;

translating at least one simulation test vector into at least one device level test vector that is in a format readable by the PLD test device; and

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results.

2. The method of Claim 1, wherein all of the simulated test vectors are translated into a corresponding device level test vector.

3. The method of Claim 1, further comprising:

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and

comparing the simulation test results with the device level test results.

4. The method of Claim 1, further comprising:

developing a software model of the programmed PLD using the design automation software tool; and

translating the software model of the programmed PLD into the simulated model of the programmed PLD using a simulation software tool.

5. The method of Claim 4, wherein the simulation software tool translates the simulation test vectors into the device level test vectors.

6. The method of Claim 5, wherein each of the device level test vectors include stimulus data and expected results data.

7. The method of Claim 1, further comprising:

generating at least one data file; and

storing each of the device level test vectors in the data files.

8. The method of Claim 7, further comprising:

compressing the data files;

storing the compressed data files on a memory storage device; and

decompressing the compressed data files to recover the device level test vectors.

9. The method of Claim 1, further comprising:

developing a software model of the programmed PLD using a design automation software tool; and

synthesizing the software model of the programmed PLD using a design synthesis software tool.

10. The method of Claim 9, further comprising:

generating a PLD program file from the synthesized software model.

11. The method of Claim 10, further comprising:

downloading the PLD program file into an integrated PLD circuit to create the programmed PLD.

12. The method of Claim 1, further comprising:

developing a software model of the programmed PLD using a design automation software tool;

synthesizing the software model of the programmed PLD using a design synthesis software tool;

translating the synthesized software model into a post-synthesis simulated model of the programmed PLD using the simulation software; and

testing the post-synthesis simulated model of the programmed PLD using each of the simulation test vectors to obtain post-synthesis simulation test results.

13. A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

developing at least one simulation test vector using PLD a design automation software tool, each simulation test vector useful for testing a simulated model of the programmed PLD;

translating at least one simulation test vector into at least one device level test vector that is in a format readable by the PLD test device;

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results;

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and

comparing the simulation test results with the device level test results.

14. The method of Claim 13, wherein all of the simulated test vectors are translated into a corresponding device level test vector.

15. The method of Claim 13, further comprising:

developing a software model of the programmed PLD using the design automation software tool; and

translating the software model of the programmed PLD into the simulated model of the programmed PLD using a simulation software tool.

16. The method of Claim 15, wherein the simulation software tool translates the simulation test vectors into the device level test vectors.

17. The method of Claim 16, wherein each of the device level test vectors include stimulus data and expected results data.

18. The method of Claim 13, further comprising:

generating at least one data file; and

storing each of the device level test vectors in the data files.

19. The method of Claim 18, further comprising:

compressing the data files;

storing the compressed data files on a memory storage device; and

decompressing the compressed data files to recover the device level test vectors.

20. The method of Claim 13, further comprising:

developing a software model of the programmed PLD using a design automation software tool; and

synthesizing the software model of the programmed PLD using a design synthesis software tool.

21. The method of Claim 20, further comprising:

generating a PLD program file from the synthesized software model.

22. The method of Claim 21, further comprising:

downloading the PLD program file into an integrated PLD circuit to create the programmed PLD.

23. The method of Claim 13, further comprising:

developing a software model of the programmed PLD using a design automation software tool;

synthesizing the software model of the programmed PLD using a design synthesis software tool;

translating the synthesized software model into a post-synthesis simulated model of the programmed PLD using the simulation software; and

testing the post-synthesis simulated model of the programmed PLD using each of the simulation test vectors to obtain post-synthesis simulation test results.

24. A method of verifying proper design and operation of a programmed programmable logic device (PLD) utilizing a PLD test device, comprising:

developing a software model of the programmed PLD using a design automation software tool;

translating the software model of the programmed PLD into a simulated model of the programmed PLD using a simulation software tool;

developing at least one simulation test vector using PLD the design automation software tool, each simulation test vector used to testing the simulated model of the programmed PLD;

translating at least one simulation test vector into at least one device level test vector that is in a format readable by a PLD test device;

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results;

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and

comparing the simulation test results with the device level test results.

25. A method of designing, implementing, and verifying proper operation of programmed programmable logic devices (PLDs), comprising:

developing a software model of the programmed PLD using a design automation software tool;

synthesizing the software model of the programmed PLD using a design synthesis software tool;

implementing the programmed PLD based on the synthesized software model;

developing at least one simulation test vector using the design automation software tool, each simulation test vector useful for testing a simulated model of the programmed PLD;

translating each simulation test vector into at least one device level test vector that is in a format readable by a PLD test device; and

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results.

26. The method of Claim 25, wherein all of the simulated test vectors are translated into a corresponding device level test vector.

27. The method of Claim 25, further comprising:

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results; and

comparing the simulation test results with the device level test results.

28. The method of Claim 25, further comprising:

translating the software model of the programmed PLD into the simulated model of the programmed PLD using a simulation software tool.

29. The method of Claim 28, wherein the simulation software tool translates the simulation test vectors into the device level test vectors.

30. The method of Claim 25, wherein each of the device level test vectors includes stimulus data and expected results data.

31. The method of Claim 25, further comprising:

generating at least one data file; and

storing each of the device level test vectors in the data files.

32. The method of Claim 31, further comprising:

compressing the data files;

storing the compressed data files on a memory storage device; and

decompressing the compressed data files to recover the device level test vectors.

33. The method of Claim 25, wherein the step of implementing the programmed PLD comprises:

generating a PLD program file from the synthesized software model; and

downloading the PLD program file into an integrated PLD circuit to create the programmed PLD.

34. The method of Claim 25, further comprising:

translating the synthesized software model into a post-synthesis simulated model of the programmed PLD using the simulation software; and

testing the post-synthesis simulated model of the programmed PLD using each of the simulation test vectors to obtain post-synthesis simulation test results.

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35. A method of designing, implementing, and verifying proper operation of programmed programmable logic devices (PLDs), comprising:

developing a software model of the programmed PLD using a design automation software tool;

synthesizing the software model of the programmed PLD using a design synthesis software tool;

implementing the programmed PLD based on the synthesized software model;

developing at least one simulation test vector using the design automation software tool, each simulation test vector useful for testing a simulated model of the programmed PLD;

translating at least one simulation test vector into at least one device level test vector that is in a format readable by a PLD test device;

testing the simulated model of the programmed PLD using each of the simulation test vectors to obtain simulation test results;

testing the programmed PLD in the PLD test device using each of the device level test vectors to obtain device level test results; and

comparing the simulation test results with the device level test results.

36. A method of translating simulation test vectors used to test a simulated model of a programmed programmable logic device (PLD) into device level test vectors used to test the programmed PLD, the method comprising:

applying at least one simulation test vector to a simulated model of the programmed PLD;

capturing a response of the simulated model to the applied simulation test vector; and

converting the simulation test vector and captured response into a format readable by a PLD test device.

37. The method of Claim 36, further comprising:

categorizing the simulation test vector as one of an input stimulus and a bi-directional stimulus; and

categorizing the captured response as one of an output response and a bi-directional response.

38. The method of Claim 36, further comprising:

outputting the simulation test vector to a predetermined file.

39. The method of Claim 38, wherein the predetermined file is one of a pull-up file, a pull-down file, a burst fault file, and a pin fault file.

40. The method of Claim 36, further comprising:

monitoring an occurrence of a rising edge of a predetermined signal; and

incrementing a counter with each occurrence of the rising edge to obtain a total count.

41. The method of Claim 40, further comprising:

outputting the total count to a count file.

42. A computer implemented system for translating simulation test vectors used to test a simulated model of a programmed programmable logic device (PLD) into device level test vectors used to test the programmed PLD, the system comprising:

means for applying at least one simulation test vector to a simulated model of the programmed PLD;

means for capturing a response of the simulated model to the applied simulation test vector; and

means for converting the simulation test vector and captured response into a format readable by a PLD test device.

43. The system of Claim 42, further comprising:

means for categorizing the simulation test vector as one of an input stimulus and a bi-directional stimulus; and

categorizing the captured response as one of an output response and a bi-directional response.

44. The system of Claim 42, further comprising:

means for outputting the simulation test vector to a predetermined file.

45. The system of Claim 44, wherein the predetermined file is one of a pull-up file, a pull-down file, a burst fault file, and a pin fault file.

46. The system of Claim 42, further comprising:

means for monitoring an occurrence of a rising edge of a predetermined signal; and

means for incrementing a counter with each occurrence of the rising edge to obtain a total count.

47. The system of Claim 46, further comprising:
outputting the total count to a count file.

48. A computer-readable storage medium containing computer executable code for instructing a computer to perform steps that translate simulation test vectors used to test a simulated model of a programmed programmable logic device (PLD) into device level test vectors used to test the programmed PLD, the steps comprising:

applying at least one simulation test vector to a simulated model of the programmed PLD;

capturing a response of the simulated model to the applied simulation test vector; and

converting the simulation test vector and captured response into a format readable by a PLD test device.

49. The storage medium of Claim 48, further comprising the steps of:

categorizing the simulation test vector as one of an input stimulus and a bi-directional stimulus; and

categorizing the captured response as one of an output response and a bi-directional response.

50. The storage medium of Claim 48, further comprising the steps of:

outputting the simulation test vector to a predetermined file.

51. The storage medium of Claim 50, wherein the predetermined file is one of a pull-up file, a pull-down file, a burst fault file, and a pin fault file.

52. The storage medium of Claim 48, further comprising the steps of:

monitoring an occurrence of a rising edge of a predetermined signal; and

incrementing a counter with each occurrence of the rising edge to obtain a total count.

53. The storage medium of Claim 52, further comprising the steps of: outputting the total count to a count file.

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